



More Moore:

Designing Ultra-Complex System-on-Chips

EPFL, Lausanne, Switzerland
22 March 2013

Workshop organized by:

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The continuing pursuit of "**Moore's Law**" in semiconductor industry for more than 40 years is presenting increasingly more significant challenges for high-complexity systems and products, including:

- Unsustainable power dissipation
- Near-atomic scale dimensions - physical limits
- Increasing process and device variability
- Diminishing performance increase with scaling
- Lack of appropriate design tools and environments
- Excessive R&D and manufacturing costs

"**More Moore**" activities aim to improve CMOS performance for the 22nm node technology and beyond. The outcomes should be applicable both in pushing forward highly scaled devices and as technology boosters that allow longer life to existing geometries.

This workshop views the design of ultra-complex system-on-chip from different angles. Three distinguished speakers from industry will present their views.

Workshop Schedule, 22 March 2013, EPFL, Room MXF1

08:45-09:00	Coffee & croissants
09:00-09:05	Opening remarks
09:05-09:45	Designing Analog/Mixed-Signal IP Beyond the 28nm Process Technology Node Joachim Kunkel <i>Synopsys Inc., California, USA</i>
09:45-10:00	Q & A Session
10:00-10:40	Trends and Challenges in Wireless SOC Design Michael Speth <i>Intel, Germany</i>
10:40-11:00	Q & A Session
11:00-11:40	More Moore: Does It Mean Mixed-Signal Integration or Disintegration? Ravi Subramanian <i>Berkeley Design Automation, California, USA</i>
11:40-12:00	Q & A Session
12:00-12:30	Panel Discussion